

TOSHIBA POWER MOS FET MODULE SILICON N & P CHANNEL MOS TYPE (L<sup>2</sup>-π-MOSIV 4 IN 1)

# MP4207

○ HIGH POWER HIGH SPEED SWITCHING APPLICATIONS.

○ H - SWITCH DRIVER

• 4-Volt Gate Drive.

• Small Package by Full Molding. (SIP 10 Pin)

• High Drain Power Dissipation. (4 Devices Operation)

$$: P_T = 4W \text{ @ } T_a = 25^\circ C$$

• Low Drain-Source ON Resistance

$$: R_{DS(ON)} = 90m\Omega \text{ TYP. (Nch)}$$

$$: R_{DS(ON)} = 170m\Omega \text{ TYP. (Pch)}$$

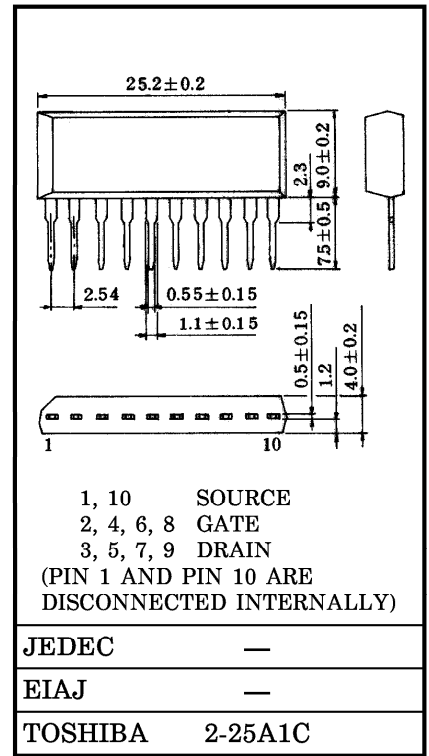
• Low Leakage Current :  $I_{GSS} = \pm 10\mu A \text{ (Max.) @ } V_{GS} = \pm 16V$

$$: I_{DSS} = 100\mu A \text{ (Max.) @ } V_{DS} = 60V$$

• Enhancement-Mode :  $V_{th} = 0.8 \sim 2.0V \text{ @ } I_D = 1mA$

**INDUSTRIAL APPLICATIONS**

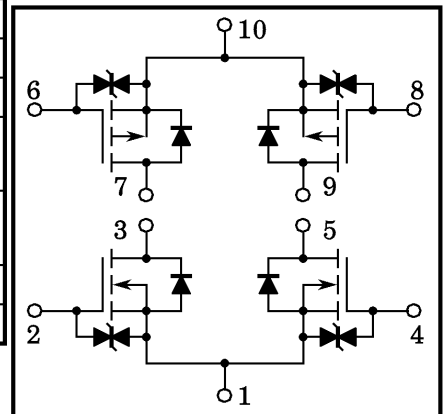
Unit in mm



**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING		UNIT
		Nch	Pch	
Drain-Source Voltage	V <sub>DSS</sub>	60	-60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	±20	V
Drain Current	I <sub>D</sub>	5	-5	A
Peak Drain Current	I <sub>DP</sub>	10	-10	A
Drain Power Dissipation (1 Device Operation, Ta = 25°C)	P <sub>D</sub>	2.0		W
Drain Power Dissipation (4 Devices Operation, Ta = 25°C)	P <sub>T</sub>	4.0		W
Channel Temperature	T <sub>ch</sub>	150		°C
Storage Temperature Range	T <sub>stg</sub>	-55~150		°C

**ARRAY CONFIGURATION**

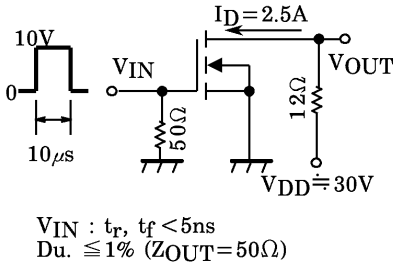


**THERMAL CHARACTERISTICS**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, Ta = 25°C)	ΣR <sub>th(ch-a)</sub>	31.2	°C / W
Maximum Lead Temperature for Soldering Purposes (3.2mm from Case for 10 second)	T <sub>L</sub>	260	°C

THIS TRANSISTOR IS AN ELECTROSTATIC SENSITIVE DEVICE. PLEASE HANDLE WITH CAUTION.

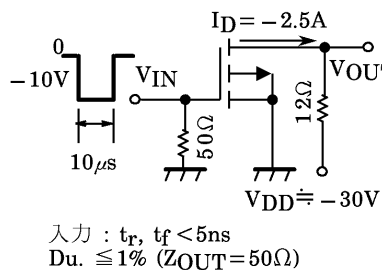
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Nch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		$I_{GSS}$	$V_{GS} = \pm 16V, V_{DS} = 0$	—	—	$\pm 10$	$\mu A$
Drain Cut-off Current		$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0$	—	—	100	$\mu A$
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$I_D = 10mA, V_{GS} = 0$	60	—	—	V
Gate Threshold Voltage		$V_{th}$	$V_{DS} = 10V, I_D = 1mA$	0.8	—	2.0	V
Forward Transfer Admittance		$ Y_{fs} $	$V_{DS} = 10V, I_D = 2.5A$	3.0	6.0	—	S
Drain-Source ON Resistance		$R_{DS(ON)}$	$I_D = 2.5A, V_{GS} = 4V$	—	135	200	$m\Omega$
Drain-Source ON Resistance		$R_{DS(ON)}$	$I_D = 2.5A, V_{GS} = 10V$	—	90	130	$m\Omega$
Input Capacitance		$C_{iss}$	$V_{DS} = 10V, V_{GS} = 0, f = 1MHz$	—	500	900	pF
Reverse Transfer Capacitance		$C_{rss}$		—	90	180	pF
Output Capacitance		$C_{oss}$		—	290	500	pF
Switching Time	Rise Time	$t_r$		—	20	40	ns
	Turn-on Time	$t_{on}$		—	60	120	
	Fall Time	$t_f$		—	80	160	
	Turn-off Time	$t_{off}$		—	300	600	
Total Gate Charge (Gate-Source Plus Gate-Drain)		$Q_g$	$I_D = 5A, V_{GS} = 10V, V_{DD} = 48V$	—	20	40	nC
Gate-Source Charge		$Q_{gs}$		—	14	—	nC
Gate-Drain (“Miller”) Charge		$Q_{gd}$		—	6	—	nC

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYPE	MAX.	UNIT
Drain Reverse Current	$I_{DR}$	—	—	—	5	A
Peak Drain Reverse Current	$I_{DRP}$	—	—	—	10	A
Diode Forward Voltage	$V_{DSF}$	$I_{DR} = 5A, V_{GS} = 0$	—	—	-1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{DR} = 5A, V_{GS} = 0$	—	140	—	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_{DR} / dt = -50A / \mu s$	—	0.4	—	$\mu C$

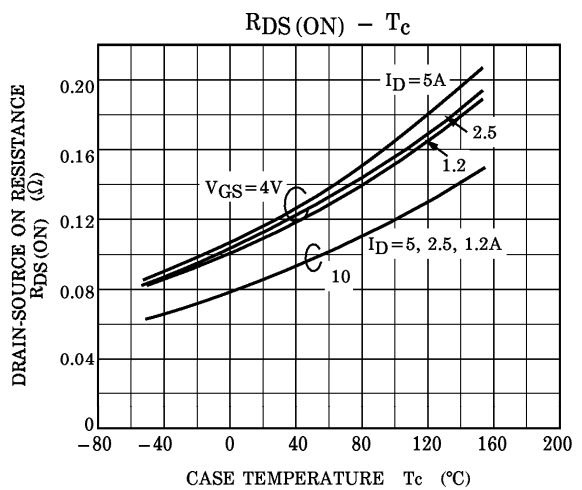
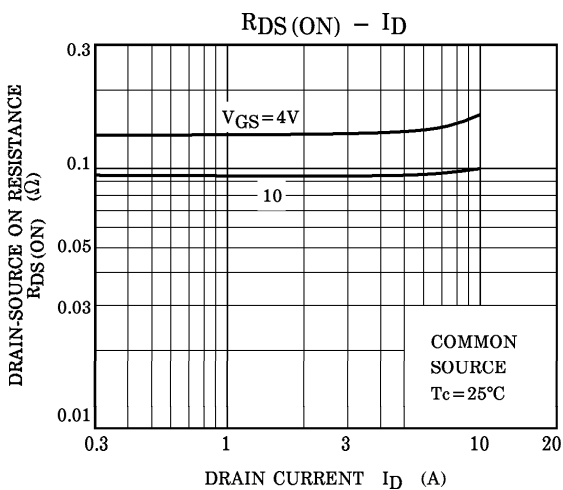
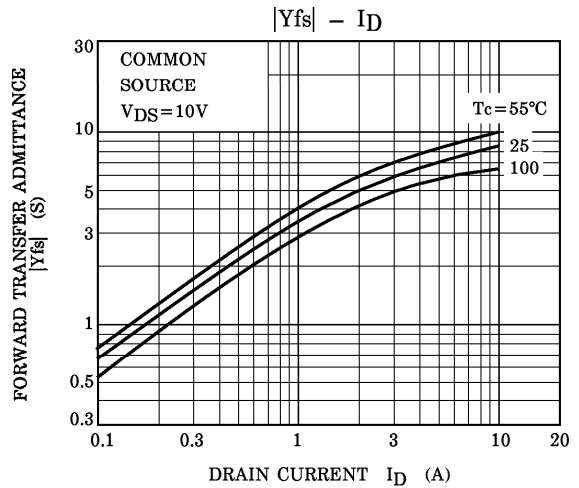
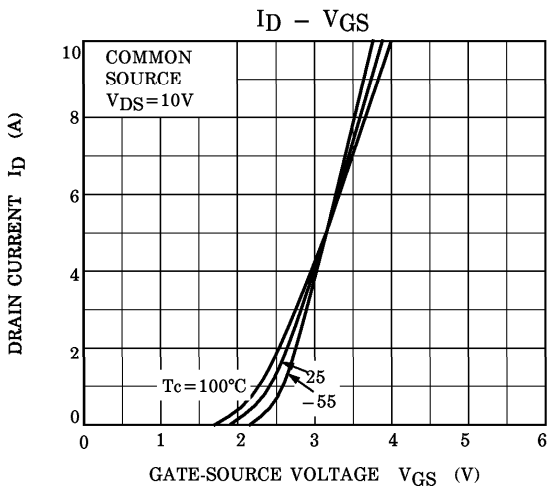
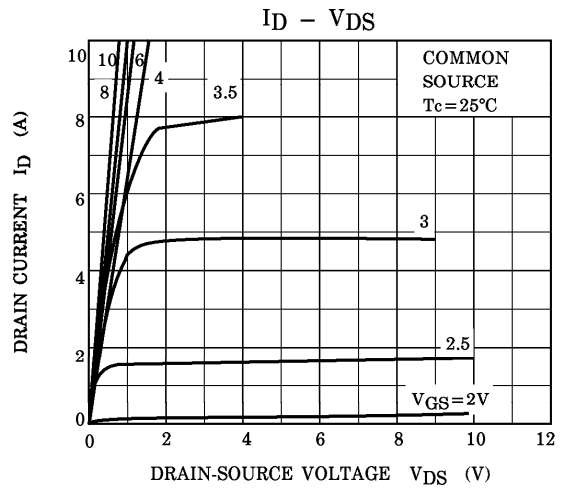
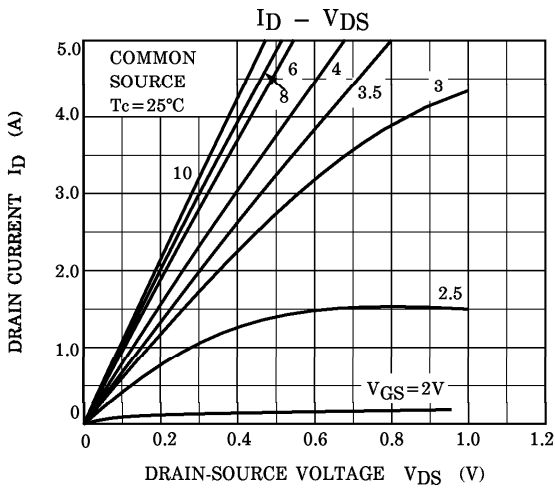
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Pch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		$I_{GSS}$	$V_{GS} = \pm 16V, V_{DS} = 0$	—	—	$\pm 10$	$\mu A$
Drain Cut-off Current		$I_{DSS}$	$V_{DS} = -60V, V_{GS} = 0$	—	—	-100	$\mu A$
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$I_D = -10mA, V_{GS} = 0$	-60	—	—	V
Gate Threshold Voltage		$V_{th}$	$V_{DS} = -10V, I_D = -1mA$	-0.8	—	-2.0	V
Forward Transfer Admittance		$ Y_{fs} $	$V_{DS} = -10V, I_D = -2.5A$	1.0	2.0	—	S
Drain-Source ON Resistance		$R_{DS(ON)}$	$I_D = -2.5A, V_{GS} = -4V$	—	250	400	$m\Omega$
Drain-Source ON Resistance		$R_{DS(ON)}$	$I_D = -2.5A, V_{GS} = -10V$	—	170	250	$m\Omega$
Input Capacitance		$C_{iss}$	$V_{DS} = -10V, V_{GS} = 0, f = 1MHz$	—	500	720	pF
Reverse Transfer Capacitance		$C_{rss}$		—	90	150	pF
Output Capacitance		$C_{oss}$		—	290	420	pF
Switching Time	Rise Time	$t_r$	 <p>入力 : <math>t_r, t_f &lt; 5ns</math>  <math>D_u \leq 1\%</math> (<math>Z_{OUT} = 50\Omega</math>)</p>	—	120	240	ns
	Turn-on Time	$t_{on}$		—	130	260	
	Fall Time	$t_f$		—	80	160	
	Turn-off Time	$t_{off}$		—	200	400	
Total Gate Charge (Gate-Source Plus Gate-Drain)		$Q_g$	$I_D = -5A, V_{GS} = -10V$ $V_{DD} = -48V$	—	22	45	nC
Gate-Source Charge		$Q_{gs}$		—	14	—	nC
Gate-Drain ("Miller") Charge		$Q_{gd}$		—	8	—	nC

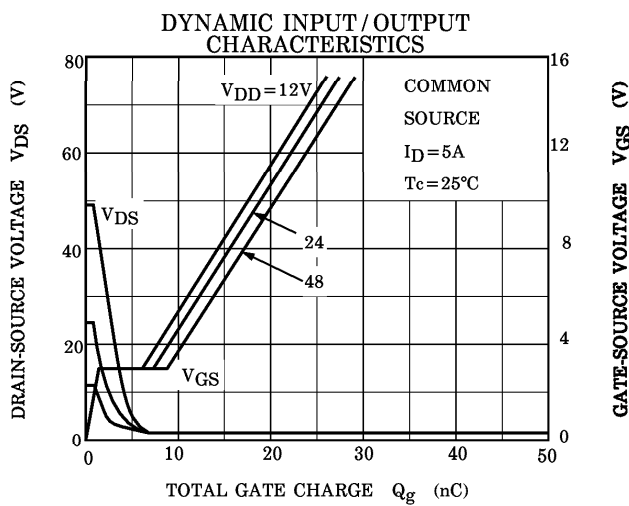
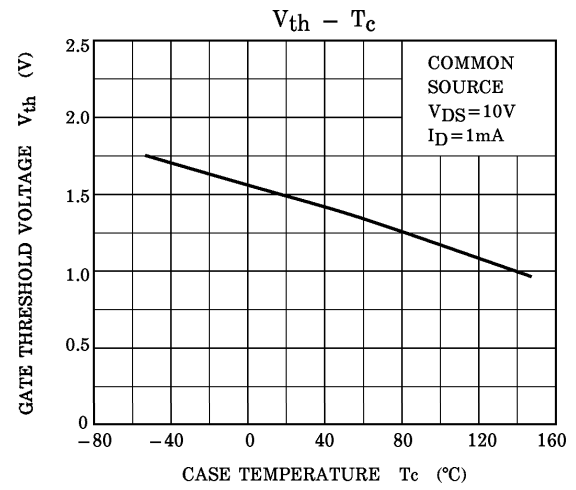
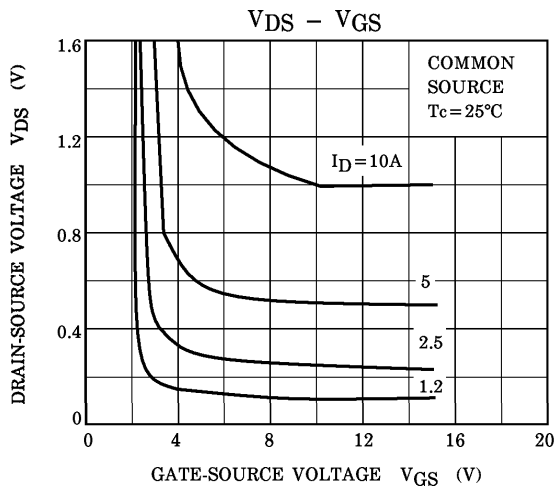
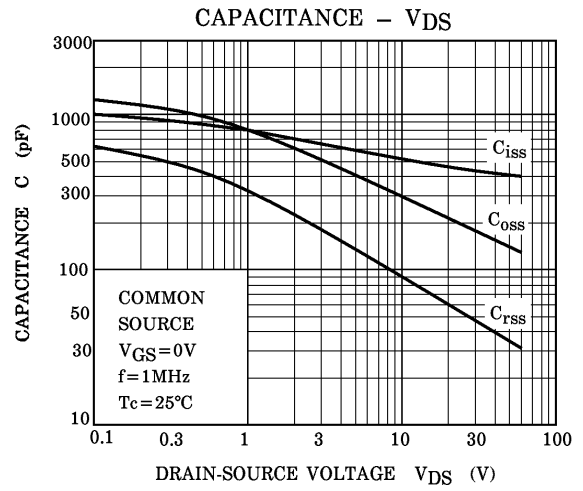
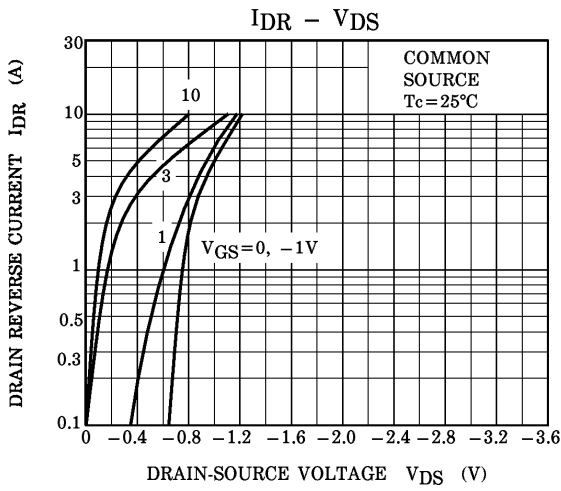
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYPE	MAX.	UNIT
Drain Reverse Current	$I_{DR}$	—	—	—	-5	A
Peak Drain Reverse Current	$I_{DRP}$	—	—	—	-10	A
Diode Forward Voltage	$V_{DSF}$	$I_{DR} = -5A, V_{GS} = 0$	—	—	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{DR} = -5A, V_{GS} = 0$	—	120	—	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_{DR} / dt = -50A / \mu s$	—	0.24	—	$\mu C$

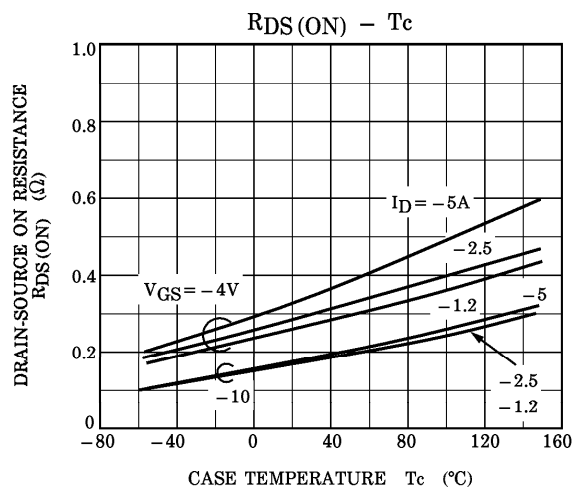
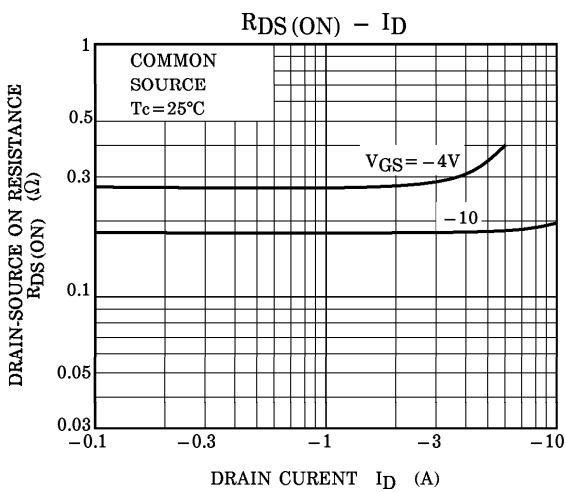
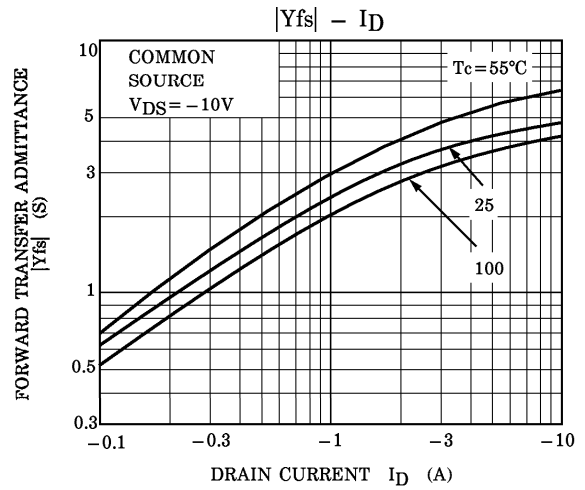
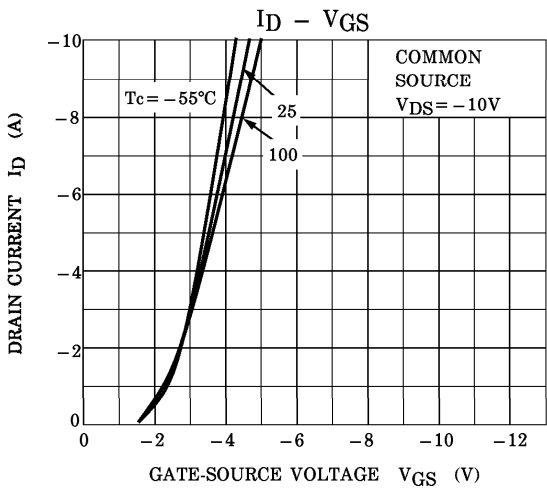
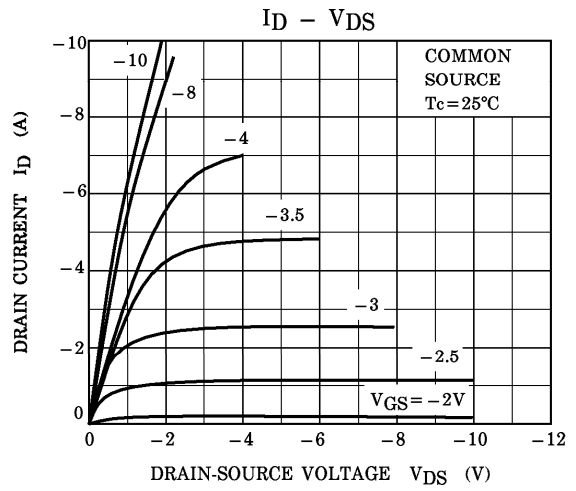
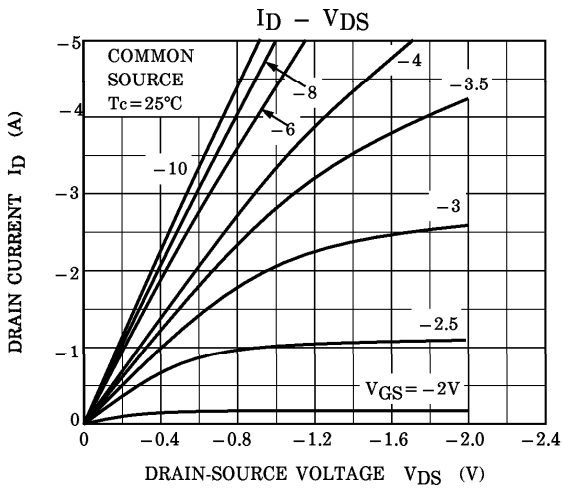
Nch FET



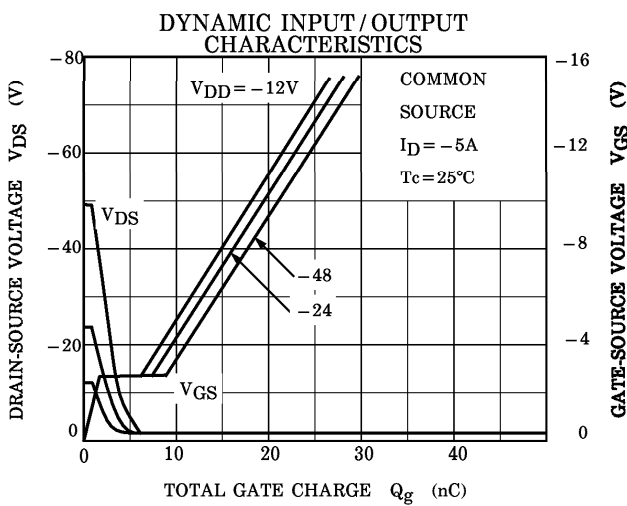
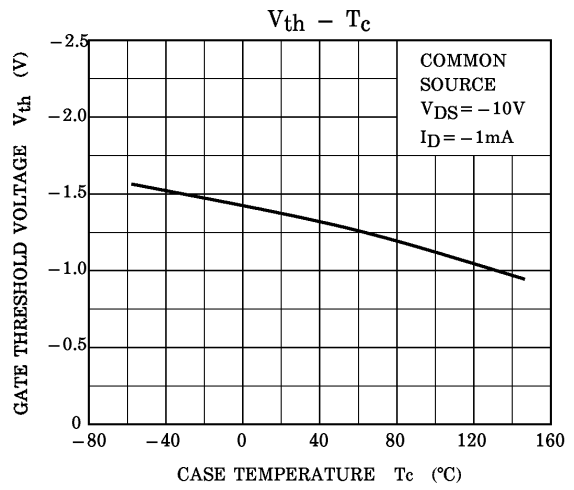
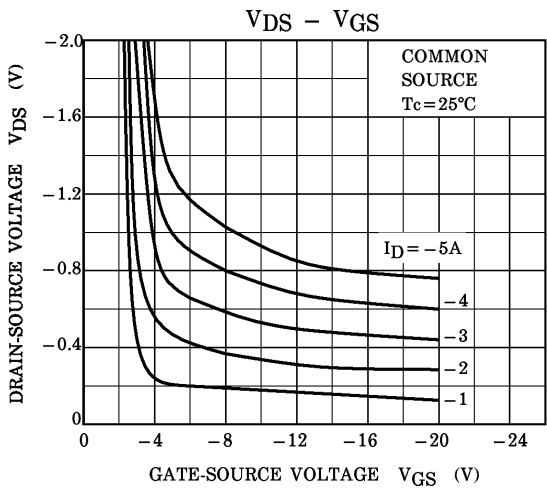
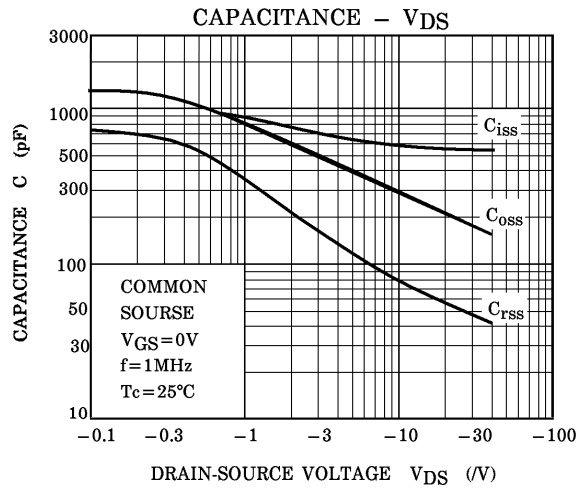
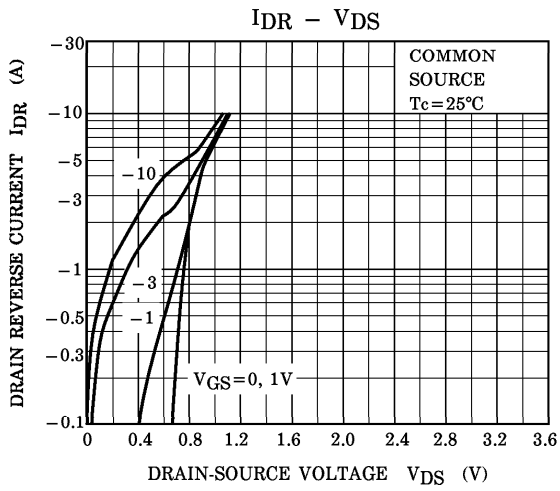
Nch FET

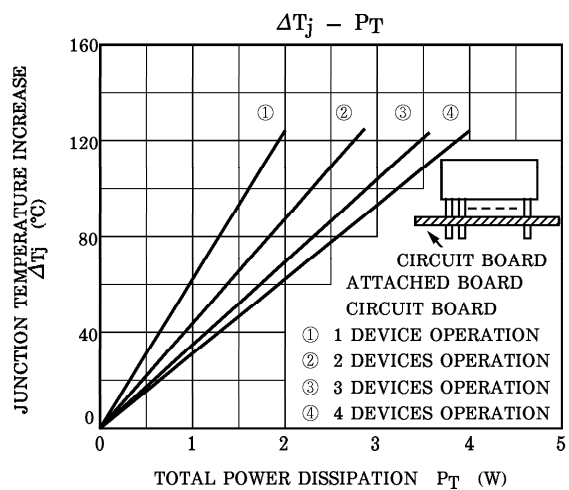
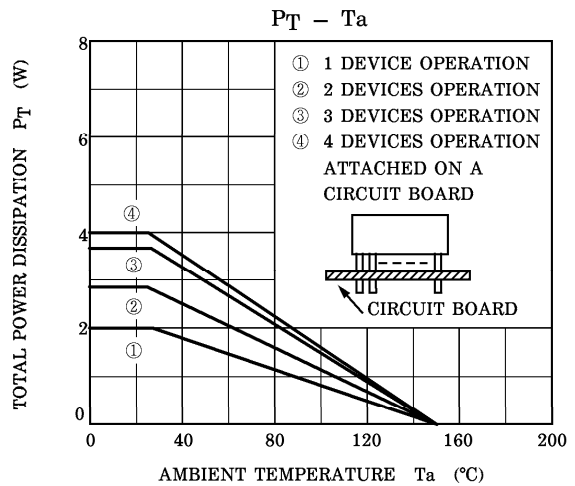
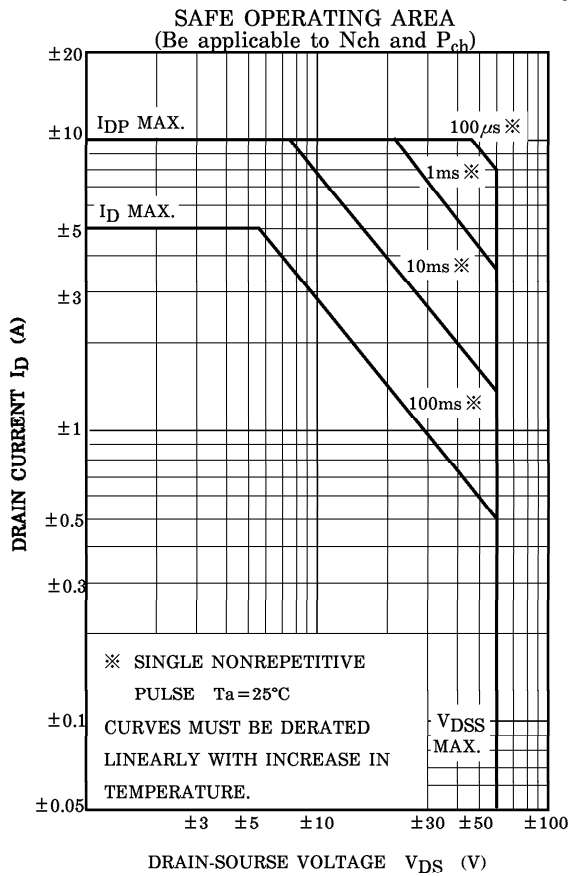
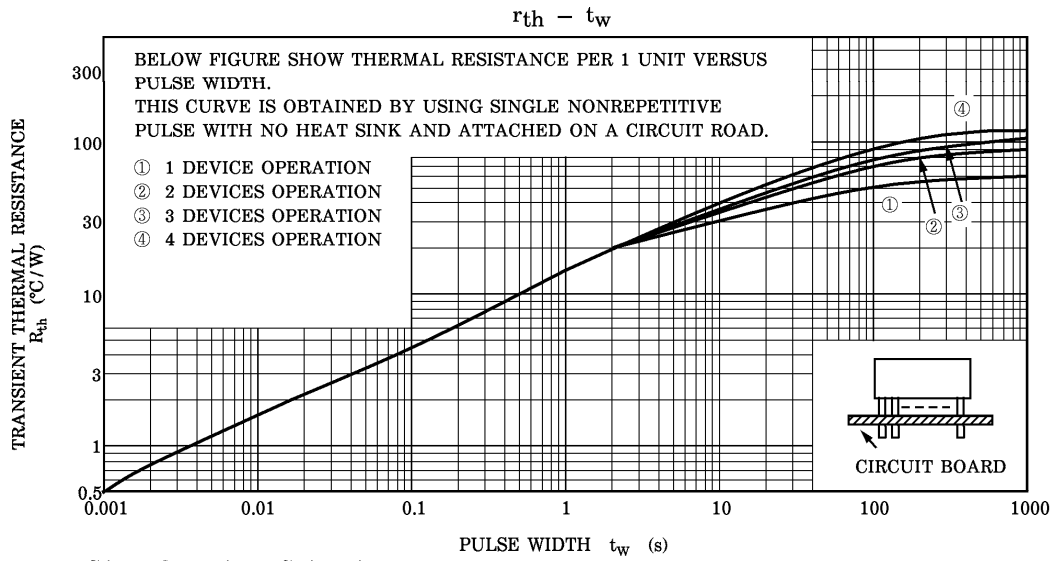


Pch FET



Pch FET







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